

TO ALL WHOM IT MAY CONCERN

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT I, Kazuhiko Tokuda, a citizen of Japan residing at Kawasaki, Japan have invented certain new and useful improvements in

PRINTED CIRCUIT BOARD WITH REDUCED CROSSTALK
NOISE AND METHOD OF FORMING WIRING LINES ON
A BOARD TO FORM SUCH A PRINTED CIRCUIT BOARD

of which the following is a specification : -

TITLE OF THE INVENTION

PRINTED CIRCUIT BOARD WITH REDUCED
CROSSTALK NOISE AND METHOD OF FORMING WIRING LINES
ON A BOARD TO FORM SUCH A PRINTED CIRCUIT BOARD

5

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to
printed circuit boards and methods of forming wiring
10 lines on boards to form such printed circuit boards,
and more particularly, to a printed circuit board
with reduced crosstalk noise generated between
adjacent two of a plurality of wiring lines spaced
thereon, and a method of forming wiring lines on a
15 board to form such a printed circuit board.

2. Description of the Related Art

A plurality of wiring lines and electronic
components are disposed on a printed circuit board,
so that a crosstalk noise will be generated between
20 adjacent two of the wiring lines which are not
sufficiently spaced. Here, the term "crosstalk
noise" refers to a noise which is generated when a
signal conducted through a signal (wiring) line is
induced by an adjacent signal (wiring) line because
25 of a coupling caused by a mutual capacitance or
inductance between the adjacent signal (wiring)
lines. When a high-frequency clock pulse is
employed as a signal, the problem of false operation
caused by such a crosstalk noise will surface.

30 For example, according to a wiring layout
on a printed circuit board 1 shown in FIG. 1, a
plurality of LSIs 2a, 2b, and 2c are connected by
means of a plurality of wiring lines. In FIG. 1,
adjacent two of the wiring lines are laid out at a
35 distance X1 from each other in a region 150,
adjacent two of the wiring lines which are disposed
so as to bypass electronic components 3a and 3b are

laid out at a distance X2-1 from each other in a region 160, and adjacent two of the wiring lines which are disposed with high density are laid out at a distance X2-2 from each other in a region 170.

5 Herein, the distance X1 is longer than the distances X2-1 and X2-2. Therefore, the noise level of a crosstalk noise generated between the adjacent two of the wiring lines laid out in the region 150 is higher than those generated between the adjacent
10 two of the wiring lines laid out in the region 160 and between the adjacent two of the wiring lines laid out in the region 170.

 In order to avoid the above drawback, a change in the wiring layout is generally made so as
15 to lengthen the distances X2-1 and X2-2, which in turn, requires a greater wiring region or multiple wiring layers.

 Hereinafter, a distance between two adjacent wiring lines is referred to as a pattern
20 pitch.

SUMMARY OF THE INVENTION

 It is a general object of the present invention to provide a printed circuit board and a
25 method of forming wiring lines on a board to form such a printed circuit board in which the above disadvantages are eliminated.

 A more specific object of the present invention is to provide a high-density printed
30 circuit board with reduced crosstalk noise and a method of forming wiring lines on a board to form such a printed circuit board.

 The above objects of the present invention are achieved by a printed circuit board including a
35 first wiring line and a second wiring line spaced apart from the first wiring line, wherein the first wiring line has first and second portions, the first

portion having a surface which faces the second wiring line and is smaller in area than that of the second portion.

5 The above objects of the present invention are achieved by a printed circuit board including a first wiring line and a second wiring line spaced apart from the first wiring line, wherein the first wiring line has a first portion having a surface which faces the second wiring line and is smaller in
10 area than a surface of the second wiring line which faces the first portion of the first wiring line.

 According to the above structures, the area of the overlapping part of the facing surfaces of adjacent two of wiring lines per unit length of a
15 wiring line can be reduced so as to reduce a crosstalk noise between the adjacent two wiring lines.

 The above objects of the present invention are also achieved by a method of forming wiring
20 lines on a board to form a printed circuit board including the steps of forming the wiring lines of a predetermined uniform thickness, and etching a first wiring line thereof so that the first wiring line has a first portion thinner than a second portion
25 thereof.

 The above objects of the present invention are also achieved by a method of forming wiring
lines on a board to form a printed circuit board including the steps of forming the wiring lines of a
30 predetermined uniform thickness, and applying a conductive material on a first wiring line thereof so that the first wiring line has a first portion thicker than a second portion thereof.

 The above objects of the present invention
35 are also achieved by a method of forming wiring lines on a board to form a printed circuit board including the steps of forming the wiring lines of a

predetermined uniform thickness, and grinding a first wiring line thereof so that the first wiring line has a first portion thinner than a second portion thereof.

5 According to the above methods, the printed circuit boards of the present invention may properly be formed.

BRIEF DESCRIPTION OF THE DRAWINGS

10 Other objects, features and advantages of the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings, in which:

15 FIG. 1 is a diagram showing a conventional wiring layout on a printed circuit board;

 FIG. 2A is a partial cross-sectional view of a printed circuit board according to a first embodiment of the present invention;

20 FIGS. 2B and 2C are partial perspective views of wiring lines formed on the printed circuit board of FIG. 2A;

 FIG. 3A is a partial cross-sectional view of a printed circuit board according to a second embodiment of the present invention;

25 FIG. 3B is a partial perspective view of wiring lines formed on the printed circuit board of FIG. 3A;

 FIG. 4 is a partial cross-sectional view of a printed circuit board according to a third embodiment of the present invention;

 FIGS. 5A through 5D are diagrams illustrating a method of forming wiring lines on a board to form a printed circuit board according to a fourth embodiment of the present invention;

35 FIGS. 6A through 6D are diagrams illustrating a method of forming wiring lines on a

board to form a printed circuit board according to a fifth embodiment of the present invention;

FIGS. 7A and 7B are diagrams illustrating a method of forming wiring lines on a board to form a printed circuit board according to a sixth embodiment of the present invention; and

FIGS. 8A through 8E are diagrams illustrating a method of forming wiring lines on a board to form a printed circuit board according to a seventh embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following, embodiments of the present invention will be described with reference to the accompanying drawings.

A description will first be given of a formula to calculate a coefficient K which indicates the amplitude of a crosstalk noise. The noise level of the crosstalk noise generated in any portion of a printed circuit board can be estimated by using the following formula. As the coefficient K becomes greater, the level of the crosstalk noise becomes higher.

$$K = (L_m / L_o + C_m / C_o) \times T_d \times 1 \times (dV / dt)$$

In the above formula, K is the coefficient to indicate the amplitude of the crosstalk noise, L_m is a mutual inductance between two adjacent wiring lines per unit length of a wiring line (unit: H), L_o is an inductance of one of the two adjacent wiring lines per unit length of a wiring line (unit: H), C_m is a mutual capacitance between the two adjacent wiring lines per unit length of a wiring line (unit: F), C_o is a capacitance of one of the two adjacent wiring lines per unit length of a wiring line (unit: F), T_d is a propagation delay time per unit length

5 Further, C_m is given as $C_m = \epsilon \times S_m / d_m$,
wherein ϵ is the dielectric constant of an
insulator between the two adjacent wiring lines, S_m
is the area of the overlapping part of the surfaces
facing each other, or facing surfaces, of the two
10 adjacent wiring lines per unit length of a wiring
line, and d_m is a distance between the facing
surfaces of the two adjacent wiring lines. Moreover,
 C_o is given as $C_o = \epsilon \times S_o / d_o$, wherein ϵ is the
dielectric constant of an insulator between the two
15 adjacent wiring lines and a GND (ground) layer, S_o
is the area of the overlapping part of the facing
surfaces of one of the two adjacent wiring lines and
the GND layer, and d_o is a distance between one of
the two adjacent wiring lines and the GND layer.

20 In the present invention, according to the
above formula, the value of K can be reduced, so as
to lower the noise level of a crosstalk noise, by
reducing L_m and C_m by setting the area S_m required
to set the level of the crosstalk noise to a level
25 equal to or lower than a desired level when other
values such as d_m , ϵ , and S_o cannot be changed,
that is, L_o and C_o remain constant.

FIG. 2A is a partial cross-sectional view of the printed circuit board 22 showing surrounding areas of a boundary between a region of a wide wiring pattern pitch and a region of a narrow wiring pattern pitch.

The printed circuit board 22 includes a

board 16 having a GND layer 12 made of a conductive material, and a core layer 14 made of a dielectric material stacked on the GND layer 12. A plurality of wiring lines 26a through 26d (or a third, a fourth, a first, and a second wiring line, respectively) made of a conductive material are disposed on the board 16, being covered with a prepreg layer 20 made of a dielectric material.

FIG. 2B is a partial perspective view of the wiring lines 26a and 26b including the portions thereof of which the cross sections are shown in FIG. 2A. FIG. 2C is a partial perspective view of the wiring lines 26c and 26d including the portions thereof of which the cross sections are shown in FIG. 2A.

As shown in FIG. 2B, the wiring lines 26a and 26b have portions of a height H2 in a region 210 (or a first and a third portion, respectively) and portions of a height H2-1 in a region 220 (or a second and a fourth portion, respectively). As shown in FIG. 2C, the wiring lines 26c and 26d have portions of a height H1 in a region 230 (or a first and a third portion, respectively) and portions of a height H1-1 in a region 240 (or a second and a fourth portion, respectively).

The wiring lines 26a and 26b, as shown in FIG. 2B, have a wider pattern pitch X3 therebetween in the region 210 than a pattern pitch X3-1 therebetween in the region 220. On the other hand, the wiring lines 26c and 26d, as shown in FIG. 2C, have a narrower pattern pitch X4 therebetween in the region 230 than a pattern pitch X4-1 therebetween in the region 240 as the wiring lines 26c and 26d are laid out with high density because of the wiring layout restricted by a plurality of wiring lines and electronic components disposed on the board 16 (see FIG. 1).

The thickness H1 of the wiring lines 26c and 26d laid out with the pattern pitch X4 in the region 230 is thinner than the thickness H1-1 of the wiring lines 26c and 26d laid out with the pattern pitch X4-1 in the region 240. This is because the noise level of a crosstalk noise between the wiring lines 26c and 26d is estimated from the above described formula to calculate K to be improperly higher in the region 230 than in the region 240 because of the narrow pattern pitch X4 according to the wiring layout if the thickness of the wiring lines 26c and 26d remain the thickness H1-1. Accordingly, the thickness H1 is set so as to obtain a desired value of K indicating a desired low noise level of the crosstalk noise therebetween in the region 230, thus allowing a high-density wiring layout therein.

On the other hand, the thickness H2 of the wiring lines 26a and 26b laid out with the pattern pitch X3 in the region 210 is thicker than the thickness H2-1 of the wiring lines 26a and 26b laid out with the pattern pitch X3-1 in the region 220. This is because the noise level of a crosstalk noise between the wiring lines 26a and 26b is estimated from the above described formula to be lower in the region 210 than in the region 220 because of the wide pattern pitch X3 according to the wiring layout if the thickness of the wiring lines 26a and 26b remain the thickness H2-1. Accordingly, the thickness H2 is set within a given range so that the noise level of the crosstalk noise will not become improperly high. The thickness H1-1 is equal to the thickness H2-1 since wiring lines are usually formed so as to have the same thickness.

According to the printed circuit board 22 having the above structure, the area Sm of the overlapping part of the facing surfaces of the

wiring lines 26c and 26d per unit length is smaller in the region 230 than in the region 240. This is because the wiring lines 26c and 26d each have the thinner thickness H1 in the region 230 than the
5 thickness H1-1 in the region 240. Therefore, a mutual capacitance between the wiring lines 26c and 26d per unit length in the region 230 is smaller than that between wiring lines of the thickness H1-1 per unit length which are laid out with the pattern
10 pitch X4. Thus, the value of K obtained from the above formula becomes a desired value small enough to lower the noise level of the crosstalk noise between the wiring lines 26c and 26d in the region 230 to the extent that no problem is incurred.

15 If the pattern pitch X4 is replaced with the pattern pitch X4-1 between the wiring lines 26c and 26d in the region 230 in the above case, the crosstalk noise therebetween will further be reduced.

On the other hand, the wiring lines 26a
20 and 26b are laid out with the wider pattern pitch X3 in the region 210 than the pattern pitch X3-1 in the region 220, and have the thicker thickness H2 in the region 210 than the thickness H2-1 in the region 220. Therefore, when the wiring lines 26a through 26d are
25 connected to make a continuous circuit, for example, increases in the resistances of the thinner portions, or the first and third portions, respectively, of the wiring lines 26c and 26d in the region 230 are offset by decreases in the resistances of the
30 thicker portions, or the first and third portions, respectively, of the wiring lines 26a and 26b in the region 210. In this case, the pattern pitch X3 may also be set as short as the pattern pitch X3-1 in the region 210 with the thickness H2 being replaced
35 with the thickness H2-1, thus allowing a high-density wiring layout in the region 210.

The above will become clearer when the

wiring lines 26a and 26c are different portions of the same wiring line, and the wiring lines 26b and 26d are different portions of the same wiring line.

5 A description will now be given, with reference to FIGS. 3A and 3B, of a structure of a printed circuit board 28 according to a second embodiment of the present invention.

10 FIG. 3A is a partial cross-sectional view of the printed circuit board 28, on which a plurality of wiring lines 32a through 32e are arranged, showing a region of narrow wiring pattern pitches. FIG. 3B is a partial perspective view of the wiring lines 32a and 32b including the portions thereof of which the cross sections are shown in FIG.
15 3A.

As shown in FIG. 3A, the wiring lines 32a through 32e are arranged on the board 16 with the pattern pitches X4, which is described in the first embodiment, in a region 310. The wiring lines 32a, 20 32c, and 32e has a thickness H3 which corresponds to the thickness H1-1 or H2-1 described in the first embodiment, and the wiring lines 32b and 32d has the thickness H1 described in the first embodiment, which is thinner than the thickness H3. That is, 25 the wiring line 32b, as well as the wiring line 32d, is formed to have a portion of the thinner thickness H1 (or a first portion) in the region 310 compared with the other wiring lines 32a, 32c, and 32e.

The wiring lines 32b and 32d are laid out 30 between the wiring lines 32a and 32c, and between the wiring lines 32c and 32e, respectively, so that each of the wiring lines having the thickness H3 will be placed adjacently to each of the wiring lines having the thickness H1.

35 Therefore, for example, the area Sm of the overlapping part of the facing surfaces of the wiring line 32a (or a second wiring line) and the

wiring line 32b (or a first wiring line) per unit length is smaller than that of the overlapping part of the facing surfaces of wiring lines of the thickness H3 per unit length which are laid out with the pattern pitch X4 (See FIG. 3B). Thus, a mutual capacitance between the adjacent wiring lines 32a and 32b is smaller than that between the above wiring lines of the thickness H3 per unit length which are laid out with the pattern pitch X4, making the value of K obtained from the above formula a desired small value. The same holds true for the other pairs of the adjacent wiring lines shown in FIG. 3A.

According to the printed circuit board 28 having the above structure, in a region wherein wiring lines are laid out with the pattern pitches X4, the noise level of a crosstalk noise generated between adjacent two of the wiring lines is lowered to the extent that no problem is incurred.

FIG. 4 is a partial cross-sectional view of a printed circuit board 100 showing a region wherein wiring lines are laid out with extremely narrow pattern pitches according to a third embodiment of the present invention.

Wiring lines 104a through 104e correspond, for example, to the wiring lines 26c and 26d of the first embodiment, and are arranged on the board 16 with extremely narrower pattern pitches X5 than the pattern pitch X4 of the first embodiment. For the convenience of a description, a wiring line L having the thickness H3 described in the second embodiment is shown by dotted lines over the wiring line 104a in FIG. 4. In this case, the wiring line 104a is formed by trimming off both shoulder portions of a wiring line having the thickness H4 slightly thinner than the wiring line L so as to have a triangular cross-sectional shape with slopes 104a1 and 104a2.

Therefore, the thickness H4 between the surface of the board 16 and a top portion 104a3 of the wiring line 104a is thinner than the thickness H3. The other wiring lines 104b through 104e have the same cross-sectional shape and slopes as the above described wiring line 104a.

The adjacent wiring lines 104a and 104b are laid out with the slope 104a2 and a slope 104b1 facing each other to form a V shape between the wiring lines 104a and 104b. Therefore, a distance dm between the slopes 104a2 and 104b1 gradually extends toward the top portion 104a3 and a top portion 104b3. Thus, a mutual capacitance between the adjacent wiring lines 104a and 104b is smaller than that between adjacent wiring lines having rectangular cross-sectional shapes which are laid out with the pattern pitch X5, making the value of K obtained from the above formula a desired value small enough to lower the noise level of the crosstalk noise between the wiring lines 104a and 104b to the extent that no problem is incurred. The same holds true for the other pairs of the adjacent wiring lines shown in FIG. 4.

According to the printed circuit board 100 having the above structure according to the third embodiment of the present invention, in a region wherein wiring lines are laid out with the pattern pitches X5, the level of a crosstalk noise generated between adjacent two of the wiring lines is lowered to the extent that no problem is incurred.

In this case, the thickness H4 between the surface of the board 16 and the top portion 104a3 of the wiring line 104a may be set as thick as or slightly thicker than the thickness H3 as far as the value of K is maintained to the desired small value. When the thickness H4 is set as thick as the thickness H3 in the above case, the wiring lines

104a through 104e can easily be formed only by trimming off both shoulder portions of the wiring line L without changing the thickness. Further, each of the wiring lines 104a through 104e may be
5 formed so as to have a trapezoidal cross-sectional shape of which an upper side is shorter than a lower side thereof remaining in contact with the surface of the board 16, instead of the triangular cross-sectional shape.

10 A description will now be given of a method of forming wiring lines on a board to form a printed circuit board according to a fourth embodiment of the present invention with reference to FIGS. 5A through 5D.

15 First, a board 38 including a core layer 36 formed on a GND layer (not shown) should first be prepared. Next, as shown in FIG. 5A, a conductive paste made of a conductive material is applied on the board 38 so as to form a conductive paste layer
20 40 thereon. Then, a mask 42 is placed on the conductive paste layer 40 so as to form a wiring pattern thereon.

Next, after an etching liquid or etchant is sprayed on unmasked portions of the conductive
25 paste layer 40, the conductive paste layer 40 is etched so that wiring lines 44a through 44d will be formed according to the wiring pattern as shown in FIG. 2B. In this case, every wiring line is formed so as to have a uniform thickness H6.

30 Then, a mask 46 is provided so that only the wiring lines 44c and 44d will be unmasked as shown in FIG. 5C. Then, each of the wiring lines 44c and 44d is etched, after the etching liquid is sprayed thereon, to have a thickness H7, which is
35 thinner than the thickness H6, as shown in FIG. 5D.

Thereby, formed is a printed circuit board 48 on which the wiring lines 44a and 44b, each

having the thickness H6, are formed with a pattern pitch X9, and the wiring lines 44c and 44d, each having the thickness H7, are formed with a pattern pitch X10, which is narrower than the pattern pitch X9. Herein, the wiring lines 44a through 44d may be referred to as a first through a fourth wiring line, respectively.

According to the above method of forming the wiring lines on the board to form the printed circuit board according to the fourth embodiment of the present invention, the printed circuit board 48 of the present invention may properly be formed.

A description will now be given of a method of forming wiring lines on a board to form a printed circuit board according to a fifth embodiment of the present invention with reference to FIGS. 6A through 6D.

As shown in FIG. 6A, a mask 52 is first placed on a core layer 50 so as to form a wiring pattern thereon. Then, a conductive paste made of a conductive material is applied, or evaporated on unmasked portions of the core layer 50 to form wiring lines 54a through 54d according to the wiring pattern as shown in FIG. 6B. In this case, every wiring line is formed to have a uniform thickness H8.

Next, a mask 56 is provided so that only the wiring lines 54a and 54b will be unmasked as shown in FIG. 6C. Then, the conductive paste made of the conductive material is applied, or evaporated on the wiring lines 54a and 54b so that the wiring lines 54a and 54b will be formed to have a thickness H9, which is thicker than the thickness H8, as shown in FIG. 6D.

Thereby, formed is a printed circuit board 55 on which the wiring lines 54a and 54b, each having the thickness H9, are formed with a pattern pitch X11, and the wiring lines 54c and 54d, each

having the thickness H8, are formed with a pattern pitch X12, which is narrower than the pattern pitch X11. Herein, the wiring lines 54a through 54d may be referred to as a first through a fourth wiring line, respectively.

According to the above method of forming the wiring lines on the board to form the printed circuit board according to the fifth embodiment of the present invention, the printed circuit board 55 of the present invention may properly be formed as in the case of the above method of forming the wiring lines on the board to form the printed circuit board according to the fourth embodiment of the present invention.

A description will now be given of a method of forming wiring lines on a board to form a printed circuit board according to a sixth embodiment of the present invention with reference to FIGS. 7A and 7B.

First, as shown in FIG. 7A, wiring lines 58a through 58d are formed according to a wiring pattern on a core layer 57 in the same method as described in the above embodiments of the present invention. In this case, every wiring line is formed to have a uniform thickness H10.

Next, each of only the wiring lines 58C and 58D is ground by using a mask or a template to have a thickness H11, which is thinner than the thickness H10, as shown in FIG. 7B.

Thereby, formed is a printed circuit board 60 on which the wiring lines 58a and 58b, each having the thickness H10, are formed with a pattern pitch X13, and the wiring lines 58c and 58d, each having the thickness H11, are formed with a pattern pitch X14, which is narrower than the pattern pitch X13. Herein, the wiring lines 58a through 58d may be referred to as a first through a fourth wiring

line, respectively.

According to the above method of forming the wiring lines on the board to form the printed circuit board according to the sixth embodiment of the present invention, the printed circuit board 60 of the present invention may properly be formed as in the case of the above method of forming the wiring lines on the board to form the printed circuit board according to the fourth embodiment of the present invention.

A description will now be given of a method of forming wiring lines on a board to form a printed circuit board according to a seventh embodiment of the present invention with reference to FIGS. 8A through 8E.

In this method, the wiring lines of the printed circuit board 100 shown in FIG. 4 are formed.

First, a conductive paste made of a conductive material is applied on the board 16 to form a conductive paste layer 110 thereon, and a mask 120 is placed on the conductive paste layer 110 so as to form a wiring pattern thereon as shown in FIG. 8A.

Next, as shown in FIG. 8B, the conductive paste layer 110 is etched according to the wiring pattern so as to form wiring lines 111a through 111c, each having the thickness H2 shown in FIG. 2B, with the pattern pitches X4 shown in FIG. 4.

Next, as shown in FIG. 8C, a mask 121 is provided so as to etch both shoulder portions of each of the wiring lines 111a through 111c. With the mask 121 being provided, portions between the adjacent two of the wiring lines 111a through 111c, and a center portion along a longitudinal center line of a top surface of each of the wiring lines 111a through 111c are masked, while the rest of the top surface of each of the wiring lines 111a through

111c, which corresponds to top surfaces of both of the shoulder portions thereof, remains unmasked.

Then, as shown in FIG. 8D, an etching process is performed for a predetermined period of time so that both of the shoulder portions of each of the wiring lines 111a through 111c will be etched, having undercuts around a top longitudinal center portion thereof.

Thereby, as shown in FIG. 8E, formed is a printed circuit board 70 on which the wiring lines 111a through 111c, each having the thickness H2 and the triangular cross-sectional shape, are formed with the pattern pitches X5.

According to the above method of forming the wiring lines on the board to form the printed circuit board according to the seventh embodiment of the present invention, the printed circuit board 70 of the present invention may properly be formed as in the case of the above method of forming the wiring lines on the board to form the printed circuit board according to the fourth embodiment of the present invention.

The present invention is not limited to the specifically disclosed embodiments, and variations and modifications may be made without departing from the scope of the present invention.

The present application is based on Japanese priority application No. 11-340815 filed on November 30, 1999, the entire contents of which are hereby incorporated by reference.